**Semiconductor nanowire unique properties**

*Out-of-plane nanowires grown by the plasma-assisted vapour-liquid-solid (VLS) method.* We develop the plasma-assisted VLS growth of silicon and germanium nanowires at relatively low temperature (400°C) using Sn, In or other non-standard catalysts. We study how such wetting catalyst materials may stay under the form of a ball, or on the contrary disappear and wet the nanowire walls¹. We analyse the evolution of the nanowire structure during growth with *ex-situ* & *in-situ* TEM. Quite surprisingly at the beginning of growth (first few minutes), a high proportion of nanowires adopts the hexagonal wurtzite-like structure with different polytypes (picture).

*High mobility in-plane silicon nanowires.* We propose prototype field effect transistors, fabricated out of SiNWs that have been grown in the plane from an amorphous silicon feedstock². Using a simple bottom-gate configuration, they exhibit a hole mobility of 228 cm²/V s and on/off ratio >10³.

*Unique thermodynamic properties.* Silicon nanowires not only adopt a normally out-of-equilibrium phase, but also accept impurity concentrations much above bulk solubilities. For Sn or In catalyzed nanowires, we find that the concentration of metal impurities in crystalline silicon increases with the growth rate and can reach a level of two orders of magnitude higher than that in their equilibrium solubility³.

For information on internships, doctoral studies, post-doctoral positions, or collaborations, please contact Jean-Luc Maurice
